DSP Systems

Project Brief

Motor Controller and Shaft Encoder

Introduction

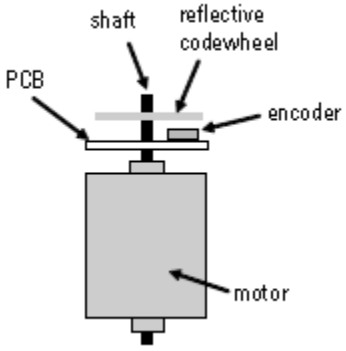
This project brief describes the design and prototype effort for a high-speed motor, motor controller, and shaft encoder hardware development project. This effort is to replace and existing controller based on an embedded Texas Instruments DSP processor using its internal analog-to-digital (A/D) converter. The design goal for the new controller is to achieve ten times the resolution and double the motor RPM. The motor hardware will be supplied by a third party vendor.

Project Approach

Initially, it was considered to use a new and faster DSP processor to accomplish the performance increase. Unfortunately the available mainstream DSPs have only a one or two mega-sample per second (MS/s), 10 or 12 bit A/D converter. This is not sufficient to accomplish the desired closed-loop control speed or accuracy. Adding an external A/D converter to a new DSP was a design option, but this approach would almost certainly require some logic between the A/D converter and signal processor hardware – complicating the design. The best approach is to use one of the new FPGA devices with a large logic fabric and hard embedded core processor – such as the Xilinx Zinq device family.

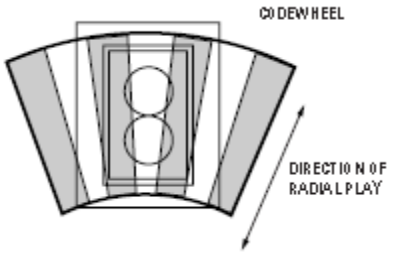
System Design

A shaft encoder is attached to the motor shaft. The encoder has and light emitting diode (LED) and photo detector so that light emitted from the LED is reflected off of a reflective code while and detected by the photo detector. The code wheel has a large number of evenly spaced lines patterned onto its outer circumference at the edge of the wheel. This is illustrated in the next few figures.



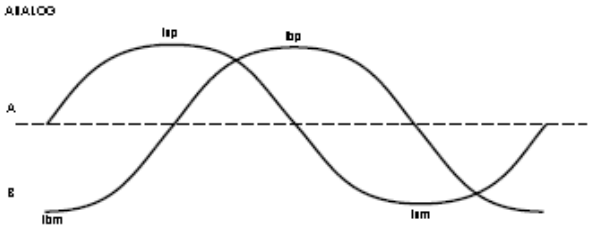
Motor with Shaft Encoder and Code Wheel Attached

This particular shaft encoder output is a quadrature signal where one phase is advanced or delayed by 90 degrees compared to the other based on the direction of rotation. This allows the controller to determine rotation rate based on the output frequency and direction based on output phases.



Code Wheel and Encoder Example

The figure above shows only one the encoder phases and does not show the index encoder that is used to determine the absolute position on the code wheel. As the shaft spins, the encoder outputs a signal similar to that shwon below. The motor controller must digitaize the signal and determine the shaft position based on the number of cycles from the index and rotation rate based on output frequency.



Encoder Output Signals

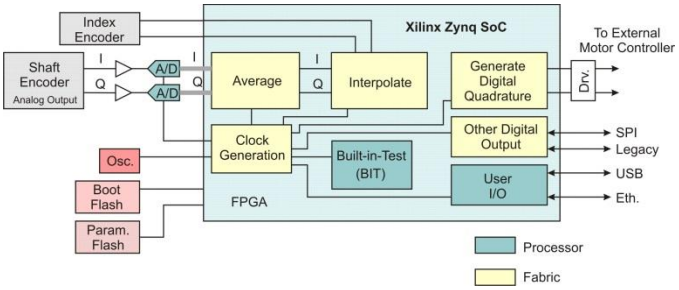
By measureing the relative amplitude of the encoder output the motor controller can actually determin its position within (or between) the code wheel line pairs using an arcsine or arctangent function. This is the goal for the project; to determine the inter line position to one part in several hunder or even one part in one-thousand.

Implementation

To achieve the design goals an external fast A/D converter with a sample rate of over 40 MS/s and sample width of 14-16 bits is required. This sample rate, or data rate, exceeds what can be accomplished using a DSP and simple memory mapped A/D converter interface. A DSP cannot reliably service an external memory mapped device at that rate (2.5ns) and do other processing and communication tasks. An FPGA device can do this.

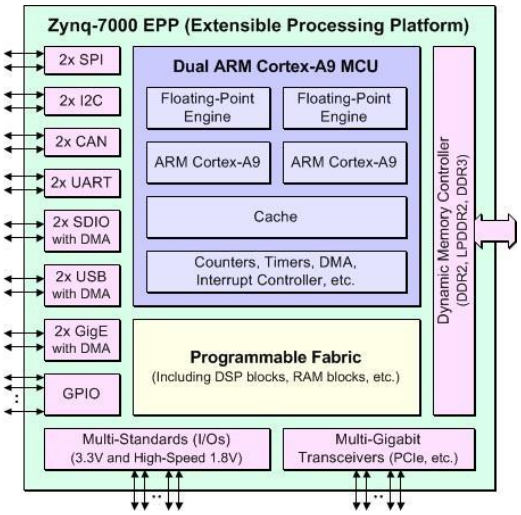
A dual-channel external 100 MHz, 16-bit converter is connected to a Xilinx Zinq system on a chip device. The Zynq has a large

logic fabric and internal memory so that the sample data can be reliabley collected and pre-processed in the ligic fabric. The Zynq also has two fast ARM processing cores with floating point capability. Though the ARM can run a real-time operating system or Linux, this application uses strictly embedded C, which seems to be refered to as bare-metal C these days.



FPGA Processing Architecture

The arcsine will be determined using a lookup table generated by the ARM processor at system startup. The FPGA will control the A/D converter, collect data, average the data, and lookup the position value. All operational perameters are programmable based on user settable rates and positional accuracy requirements which are different for each job.



Xilinx Zynq ARM Core Architecture

The Zinq ARM processor has a wide variety of built-in hardware cores attached to it making communication to the system controller or outside world relatively easy. DSP System has coded bare metal USB drivers and communications software as well as bare metal Ethernet drivers and communication software for this device.

The built-in serial peripheral controller (SPI) hardware core of the ARM processor will be used to control the external A/D converter and a diagnostic and built-in-test (BIT) port is available through the hardware UART.

Summary

This is an example of the capabilities and services available from DSP Systems. It illustrates how DSP Systems can help with your next project. If you have something that you need engineering or systems design help with, we can be of service. Give us a call.

DSP Systems specializes in developing engineering solutions for commercial and industrial applications, research and development projects, and military application problems. We will supply systems engineering, electrical design engineering, circuit card design and production engineering expertise, as well as software and firmware coding specialists to complete your entire project or work with your team to assist with any part of your next development effort.